said heavily doped grid being ohmically connected to said second power electrode.

2. The semiconductor device of claim 1 wherein said substantially planar arrangement overlaps a portion of said first region.

3. The semiconductor device of claim 1 wherein a portion of said grid is spaced from said first region by said second layer.

4. The semiconductor device of claim 1 wherein a portion of said grid is coupled to said first region.

5. The semiconductor device of claim further comprising a grid electrode disposed in ohmic contact with said grid region and connected to said second power electrode.

6. The semiconductor device of claim 1 wherein said first region comprises a shallow shelf portion of one type conductivity and a heavily doped deeper central portion of one type conductivity.

7. The semiconductor device of claim 1 wherein said grid includes a heavily doped portion which is separated from the first region by said second layer.

8. The semicoductor device of claim 7 wherein said heavily doped portion is disposed beneath said second region.

9. The semiconductor device of claim 1 wherein said first layer comprises a heavily doped zone.

10. The semiconductor device of claim 1 further including a third electrode in ohmic contact with said first layer.

11. The semiconductor device of claim 1 wherein said first region has a width L_b in a first direction substantially parallel to said first surface and each of said grid segments, has a width L_g less than or equal to 0.25 L_b in said first direction.

12. The semiconductor device of claim 1 wherein said grid has a total volume equal to approximately 75% of the total volume of the first region.

13. The semiconductor device of claim 2 wherein said first region provides said ohmic connection between said first power electrode and said grid.

14. The semiconductor device recited in claim 1 wherein said device has only three external terminals, a first terminal connected to said first power electrode, a second terminal connected to said second power electrode and the third terminal connected to said gate electrode.

15. An insulated gate semiconductor device comprising:

a body of semiconductor material including:

a first layer of one type conductivity,

a second layer of opposite type conductivity disposed atop said first layer,

a third layer of said one type conductivity disposed atop said second layer,

a first region of opposite conductivity within said third layer,

a second region of one type conductivity disposed within said first region,

said body having a first surface to which said third layer, said first region and said second region extend, and

a heavily doped grid of opposite type conductivity disposed within said third layer and spaced from said first surface for establishing a current path for opposite type conductivity carriers, said grid comprising a plurality of segment of opposite type conductivity disposed in a substantially planar arrangement and a plurality of apertures therebetween each occupied at least in part by a portion of said one type conductivity third layer, at least one of said grid segments and at least one of said grid apertures in projection on said first surface extending into a projection of said first region on said first surface;

a first power electrode disposed in ohmic contact with said first layer;

a second power electrode disposed in ohmic contact with said first and second regions; and

an insulated gate electrode disposed on said first surface over a portion of said first region for, in response to an appropriate bias potential, establishing a channel through said first region between said third layer and said second region for facilitating the flow of opposite type conductivity carriers between said third layer and said second region;

said heavily doped grid being ohmically connected to said second power electrode.

16. The semiconductor device recited in claim 15 wherein said device has only three external terminals, a first terminal connected to said first power electrode, a second terminal connected to said second power electrode and third terminal connected to said gate electrode.

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